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THE EFFECTS OF MULTIPLE-GATED LAYOUT ON POWER CONSUMPTION OF PSEUDOMORPHIC-HEMTS

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Abstract A study of the effects on power consumption exhibited by multiple-gated layout pseudomorphic HEMTs device is presented here. This study required that the DC parameter extraction to be carried out on the p-HEMT device with a specific number of gate layouts. From the I-V measurement, it was found that the p-HEMT that applied six gated layout can reduce 75% of power consumption as compared to two gated layout in producing the same amount of I_{ds}. This result proved that the p-HEMT device with higher number of gates consumes less power. The consequences of this lead to the reduction of device power consumption without sacrifying the device performance.

Introduction

The demand on the higher performance analog RF transistor device in a circuit application has led to the production of very competitive design which mainly focused on electrical characteristic improvement especially on output current, linearity, threshold voltage that gives better and higher device performance (Xu *et al.*, 1998; Bonkee *et al.*, 2000; Bonkee *et al.*, 2001; Tae *et al.*, 2004). One of the solutions to achieve this objective is by applying the multiple gated-layouts in the transistor device structure. Some researchers have done the simulation and modeling on this multiple-gated layout and found significant improvement on electrical performance of certain transistor device (Iniguez, 1999; Hon-Sum *et al.*,). Other researchers have also found that this multiple-gated layout also could also improve the power consumption of a transistor device and thus made the circuit more efficient (Chang *et al.*, 2000; Dao, 2004). However, the application of this multiple-gated concept to all semiconductor devices has not been fully explored especially for pseudomorphic HEMT (p-HEMT) device. Due to the different structure, material and operation of p-HEMT device, this concept needs to be investigated further. In this study, the effect of multiple-gated layout on power consumption performance in GaAs based p-HEMT device was observed. The result obtained from the I-V measurement will be used in the power consumption analysis.

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Material and Methods

In order to study the multiple-gate layout effect on p-HEMT device power consumption, specific layout have been used. Three types of layouts were used in this experiment, comprising of 2x60, 4x75 and 6x150 layouts. The 2x60 layout represented 2-gated layout with 60-micron gate length, and the 4x75 and 6x150 layouts represented 4-gated and 6-gated with 75 micron and 150 micron

gate width respectively. The gate length of all devices was 0.5 micron. The figure of those device layouts is shown in Fig. 1.

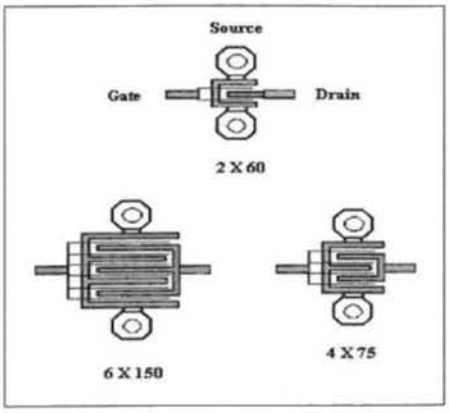

Figure 1. The layout of 2x60, 4x75 and 6x150 of p-HEMT device

Basically, the layout consists of Gate, Source and Drain terminals which are standard for p-HEMT device. The Gate terminal indicates the input and the Drain is the output terminal. In this study, the Source was connected to the common Ground at the bottom of the wafer. In other studies, the gate width for each layout was fabricated for different length. However, this variation of gate width might contribute to the performance of the device in a different way. Xu *et al.*, (1998) found that the 4x25 layout produced poorer pinch-off characteristic compared to 2x50 layouts. Even though the total gate width is the same, they show a different performance in electrical characteristic.

The on-wafer DC probing technique was the selected measurement setup used throughout the process of extracting the I-V characteristic. This technique was selected because the device was in a wafer form. The low parasitic GSG probe tips were used to probe on the device layout, which was ready in a GSG pad. One tip was probed on the Gate terminal that supplied the V_{gs} and the other tip was probed on the Drain terminal for V_{ds}. The source terminal was grounded by the chuck of the probe station. Both probe tips were connected to the Keithley Source Measure Unit (KSMU). The current flow in the device was then feedback to the analyzer to obtain the I-V characteristic of the device during the present of biasing. The basic setup for the DC measurement of p-HEMT device is shown in Fig. 2.

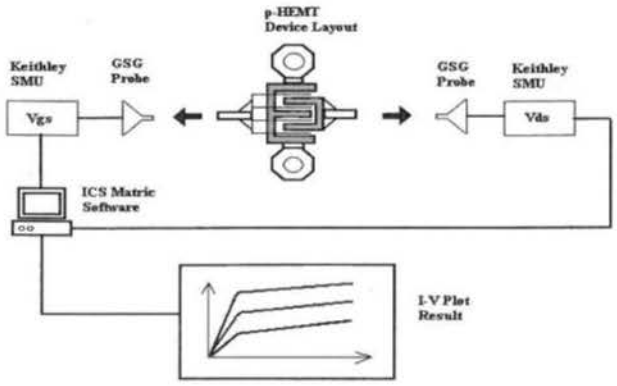

Figure 2. Setup during dc measurement of p-HEMT device

For the voltages setting, the drain-source voltage, V_{ds} was swept from 0 V to 2 V. The gate-source voltage, V_{gs} was stepped from -0.2 V to +0.2 V with the step size of 0.1 V. All the voltage settings were controlled through interactive characterization software (ICS) matrix, which communicated to the KSMU using GPIB cable. The plot of the result was being monitored on the plot windows of this ICS matrix software. All device layouts were supplied with the same voltage settings. The I_{ds} vs V_{ds} curve of each device layout was plotted accordingly.

Results and Discussion

The plot of I-V characteristic of all p-HEMT device layouts are compared at V_{gs} = 0V as shown in Fig. 3.

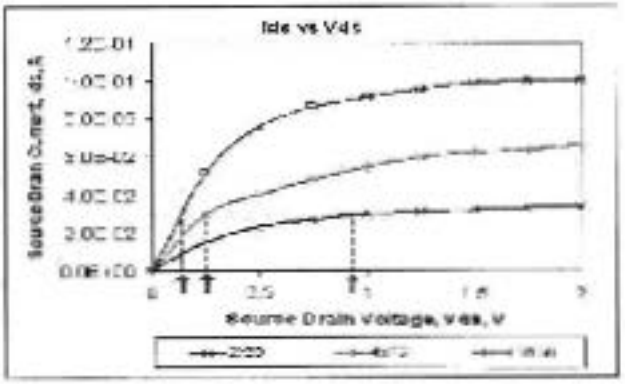

Figure 3. I_{ds} vs V_{ds} at V_{gs} = 0 V

From Fig. 3, it can be observed that the 6x150 layout produced higher source-drain current as suggested by Mohd Nizam et al., (2006). The horizontal dotted line on the plot shows a constant 30 mA I_{ds} current and the vertical dotted lines show the corresponding V_{ds} required for each layout in order to produce that amount of current. It was found that the 6x150 layout required only 0.13 V of biasing voltage while the 4x75 and 2x60 layouts required 0.26 V and 0.85 V respectively. The calculation of device power consumption P is given by (1):

$$P_{static} = V_{ds} \times I_{ds} \quad \text{..... (1)}$$

From (1), the calculation of power consumption given by 6x150 layouts to produce 30 mA I_{ds} at V_{gs} = 0 V was about 4 mW. Meanwhile the 4x75 and 2x60 were 7.8 mW and 25.5 mW respectively. Therefore, the higher number of gate layout consumed less power in producing the same drain-source current, I_{ds}. In comparison, 6x150 reduced power consumption more than 50% to that of 4x75 and 75% to that of 2x60 layout. As shown in Fig. 4, the plot was obtained at slightly positive value of V_{gs} = 0.2 V. It shows that the curve given by 6x150 was already saturated to 100 mA due to equipment limitation. However, in order to produce 40 mA Ids, the 6x150 layout only required 0.16 V with power consumption of 6.4 mW, while the 4x75 and 2x60 required 0.32 V and 1.0 V with power consumption of 12.8 mW and 40 mW respectively. Again the 6x150 layout significantly reduced about 50% compared to that of 4x75 and about 75% to that of 2x60.

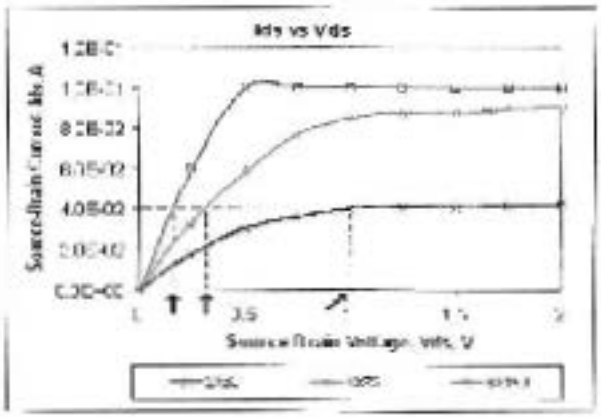

Figure 4. I_{ds} vs V_{ds} at $V_g = 0.2$

For the negative V_{gs} the plot of the drain-source current is given in Fig. 5 at V_g = -0.2 V. The purpose of this setting was to observe the consistency of the power consumption at any range of gate bias. As from (1), the power consumption of 6x150 was about 3.2 mW in order to produce 20 mA I_{ds}. Meanwhile the 4x75 and 2x60 consumed 6.4 mW and 20 mW respectively. With the reduction of about 50% in 4x75 layout and 75% in 2x60 layout, the results indicated the consistency of the power consumption reduction of 6x150 layout at any range of bias voltage. The same percentage of power consumption reduction was obtained regardless of the range of I_{ds} and V_{ds}.

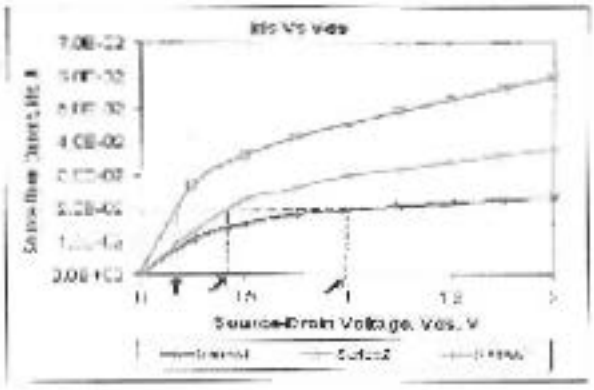

Figure 5. I_{ds} vs V_{ds} at $V_g = -0.2$ V

Based on previous current voltage relationship, the general plot of power consumption and the ids current for each layout is illustrated in Fig. 6. Figure 6 shows that the power consumed by 2-gated layout is greater than the 4-gated and 6-gated layouts at any point of I_{ds}. The extrapolation of the 2-gated layout (shown by dotted line) is carried out in order to demonstrate the differences in power consumption by the outlets.

Another comparison on the relationship between the power consumption and the number of gates is illustrated in Fig. 7. From Fig. 7, it is clearly observed that as the number of gate increases, the power consumption decreases, and even lower at smaller value of I_{ds}.

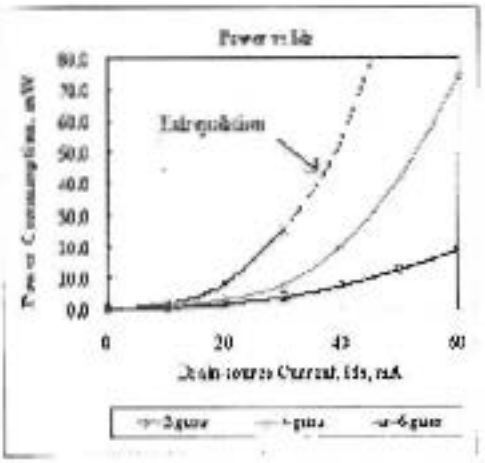

Figure 6. Power vs I_{ds} at V_g –0 V

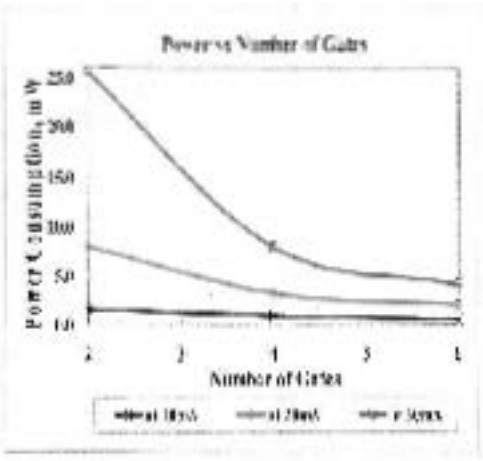

Figure 7. Power vs no. of gates

Conclusion

By measurement, it was proven that multiple-gated layout applied in p-HEMT device was the best procedure to solve high power consumption problem in circuit design. The higher the number of gates, the more power would be reduced significantly. This finding also supported the common understanding regarding the advantage of multiple-gated layout as obtained in other semiconductor device like FET, MESFET and MOSFET. The capability of multiple-gated layout p-HEMT device in reducing quite a big percentage in power consumption while maintaining the performance makes this concept applicable to most RF circuit systems.

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References

Benjamin Iniguez, 1999. IEEE Trans. On Electron Device 46(8):1742-1748.

Bonkee Kim, Ho-Su Ko and Kwyro Lee, 2000. IEEE Microwave and Guided Wave Letters 10(9):371-373.

Bonkee Kim, Jin Su-Ko and Kwyro Lee, 2001. IEEE MTT-S Digest 5.5-518 pp.

Chang, E. Y., D. Kuang Lee, S. H. Chen and T. C. Chang, 2000. Electronics Letters 36(6): 575-579.

Hon-Sum Philip Wong, David J. Frank and Paul M. Solomon, IBM T. J Watson Research Center, Yorktown Heights, New York 10598, USA. 407-410 pp.

Mohd Nizam, O., A. Zaki, Y. Syamsul, Y. Mohamad Rasman and A. M. Abdu' Razak, 2005. In Proc. Proceeding of IEEE International Conference on RF and Microwave.

Tae Wok Kim, Bonkee Kim and Kwyro Lee. 2004. IEEE Journal of Solid State Circuits 39(1):223-229.

Tury Dao. 2004. In Proceeding of IEEE International Conference on Integrated Circuit Design and Technology 99 pp.

Xu, D., T. Enoki, T. Suzuki, Y. Umeda, Y. Yamane and Y. Ishii. 1998. Electronics Letters 34(16):16.4-1615.